Carry & Overflow Detection

Byte addition:

$S_7S_6S_5S_4\,S_3S_2S_1S_0$ = $A_7A_6A_5A_4\,A_3A_2A_1A_0$ + $B_7B_6B_5B_4\,B_3B_2B_1B_0$

A_7	B_7	S_7		V		C
0	0	0		0		0
0	0	1		1		0
0	1	0		0		1
0	1	1		0		0
1	0	0		0		1
1	0	1		0		0
1	1	0		1		1
1	1	1		0		1

2-level AND-OR Implementation

Gate inputs, top to bottom order: A_7, B_7, S_7